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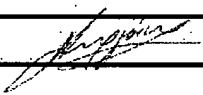
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	First Named Inventor	Krinder, Jason D.
	Art Unit	2134
	Examiner Name	Malven, Andrew L.
	Attorney Docket Number	TI-29077
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MAY 09 2006

In re the Application of:

Docket No.: TI-29077

Jason D. Krinder

Art Unit: 2134

Serial No: 09/712,873

Examiner: Nalven, Andrew L.

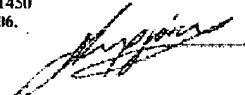
Filed: November 15, 2000

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For: Authorization Control Circuit and Method

May 8, 2006

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REPLY BRIEF

Dear Sir:

This reply brief is filed in response to the Examiner's Answer dated March 8, 2006, which was issued in response to the Applicants' appeal brief.

REPLY ARGUMENTS

1 of 5

- a) Seo teaches away from a digital-to-analog converter receiving a disable signal and muting the output of the digital-to-analog converter in response to the disable signal

In the Examiner's Answer, the Examiner states that the Seo reference does not teach away from the present invention. Applicants respectfully disagree.

MPEP § 2145(X)(D)(2) states, "It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)" MPEP § 2141.02(VI) states, "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)"

Applicants reiterate that the Examiner mistakenly states that Seo teaches a digital-to-analog converter ... operable to ... mute the output of a corresponding analog data in response to a disable signal (see page 3 of Final Rejection). Seo, as previously stated in the appeal brief, teaches a first switching circuit that receives a mute control and a first digital data from a DSP and a fourth digital data from a multiplier. The first switching circuit then selects and outputs selectively the first or the fourth digital data to a digital-to-analog converter (Seo column 3, lines 32-38). The Examiner mistakenly states that the digital-to-analog converter receives the disable signal and mutes the output of the corresponding analog data in response thereto. In addition, the first switching circuit does not selectively output a muted signal or a non-muted signal as the Examiner states. As stated above, the first switching circuit selects between the first and the fourth digital data.

The Examiner states that in *Syntex v. Apotex* the court noted that “a prior art reference that does not specifically refer to one element of a combination does not, per se, teach away” (*Syntex v. Apotex*, page 15). Seo, however, does not merely omit a reference to an element. Seo specifically teaches connecting the disable signal to a different unit and not to the digital-to-analog converter. The MPEP states that it would be improper to combine references that teach away from their combination. Outputting the disable signal directly to the digital-to-analog converter is substantially different from outputting the disable signal to another device that is operable to receive one of two signals and select one to output to the digital-to-analog converter. Much more functionality may be added to the digital-to-analog converter, for example, by the digital-to-analog converter’s direct reception of the disable signal.

The Examiner also stated that the court further noted, “a statement that a particular combination is not a preferred embodiment does not teach away absent clear discouragement of that combination” (*Syntex v. Apotex*, page 15). There is no such statement in Seo, however. Applicants respectfully ask the Examiner to identify the part in Seo where a particular combination is identified as not a preferred embodiment. Seo teaches away from the claimed combination by specifically teaching to send the disable signal to a unit other than the digital-to-analog converter. The MPEP states that a prior art reference must be considered in its entirety, including portions of the reference that may contradict or teach away from the invention or from teachings of other references.

- b) Examiner stated that Seo teaches a digital-to-analog converter operable to receive a disable signal and disable the output in response to the disable signal

The Examiner also states that the Examiner did not rely on the Seo reference to teach the digital-to-analog receiving a disable or mute signal. In the final rejection and again in the Examiner's answer, however, the Examiner states: "DeLuca fails to teach a digital to analog converter operable to receive the disable signal Seo teaches a digital to analog converter (Seo, column 3 lines 32-38) coupled to a digital signal processor and operable to receive the digital data output (Seo, Figure 4 Items 41 and 40), convert the digital data to corresponding analog data (Seo, column 3 lines 32-38), output the corresponding analog data (Seo, column 3 lines 32-38, Figure 2C), mute the output of the corresponding analog data (Seo, column 3 lines 32-38), *receive the disable signal (Seo, column 3 lines 32-34), and mute the output of the corresponding analog data in response to the disable signal (Seo, Figures 2B and 2C, column 3 lines 14-38)*" (emphasis added). The Examiner clearly states that, in the Examiner's belief, Seo teaches a digital-to-analog converter operable to receive a disable signal and mute the output in response to the disable signal. In addition, this statement preceded any statement by the Examiner that Nagata teaches a digital-to-analog converter operable to receive the disable signal. Applicants assumed, therefore, that it was the Examiner's belief that Seo was being used as a reference against that element. Applicants, therefore, suggest that the Examiner withdraw the above statement if the examiner does not believe the above statement to be true.

- c) The Examiner has failed to establish a reasonable expectation for success in combining DeLuca, Tran, Seo, and Nagata

Applicants reiterate that the reasonable expectation of success criterion of MPEP 2143 has not been met since the absence of all the recited claim limitations and the

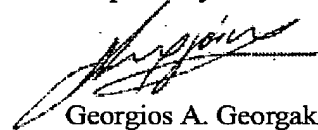
presence of references that teach away from the present invention preclude any reasonable expectation of success. Consequently, this criterion also is not met by the Examiner.

Conclusion

For the reasons set forth above, Applicants respectfully submit that Claims 1-23 are patentable over DeLuca, Seo, Tran, and Nagata. Accordingly, Applicants pray that the Honorable Board will reverse the Primary Examiner's rejection of Claims 1-23.

The Commissioner is authorized to charge any fees that may be associated with this reply brief to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



Georgios A. Georgakis
Attorney for Applicants
Reg. No. 46,723

Robert D. Marshall, Jr.
Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5290